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DESIGN OF LOW NOISE AMPLIFIER USING CMOS LOGIC

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Abstract-
The main important aspect in a Communication system is a Receiver. If receiver receives weak signals from an antenna makes communication system be weaker Due to improved parameters like gain, noise, bandwidth, linearity, chip area and power consumption of a Low noise Amplifier (LNA) makes receive part be an efficient for amplification. The pre and post simulation waveforms obtained for transient analysis and AC analysis. This Project is designed an efficient LNA with very low voltage supply as well as it provides high gain and bandwidth with a small chip area occupancy. This will make receiver section in communication part be strong in amplification.
We want to design the CMOS system by using EDA tool.
Keywords: LNA, optimization, PDP

Introduction:

An amplifier will increase the power of both signal and noise present as its input, but the amplifier will also introduce some additional noise, A low-noise amplifier(LNA) is a electronic amplifier that amplifies a very low-power signal without significantly degrading its signal to noise ratio. Actually LNA's designed to minimize that additional noise.so Designers can minimizing additional noise by choosing low noise components, operating points and circuit topologies. Today, demand for mobile wireless communication devices and high-speed computer equipment is growing on the market.

This goes without saying that the low cost and high performance of integrated WLAN circuits have contributed to commercial success. However, these devices have only a limited battery life. Battery systems with electronics have not changed. Since upgrades to batteries do not meet the demand for wireless equipment, innovative circuit design technologies need to be developed in order to reduce energy use and use low power. Basic building blocks of mobile wireless communication the use of manufacturing technology is very important for the implementation and development of these circuits.
Low Noise Amplifier (LNA) design considerations are low noise figure, good input and output matching, high gain, stability and linearity. Although these considerations are crucial, they are

Catalyst Research Volume 23, Issue 2, September 2023 Pp. 1165-1171

interdependent and to find a common optimum solution is not easy. To satisfy these considerations, transistor selection is one of the most important step in LNA

Design.

Existing Method:

The LNA includes a CS & CG amplifier stages The NC technique is adopted to decrease the noise involvement of the amplifier. Compared with CS, in the interim, the power gain & the total NF performances are also improved further. It has been experiential that the proposed LNA's linearity has little effect on the CG path . Consequently, the bias voltage of the circuit and power consumption is optimized to reduce in the path. The different noise cancellation of paths for CMOS LNAs goes during bring in a phase mismatch among the 2 parallel paths. This phase mismatch harmfully impacts the system noise cancellation &gain . For that reason, its cause on performance of NF and gain is furthermore quantitatively with analyzed in this paper.

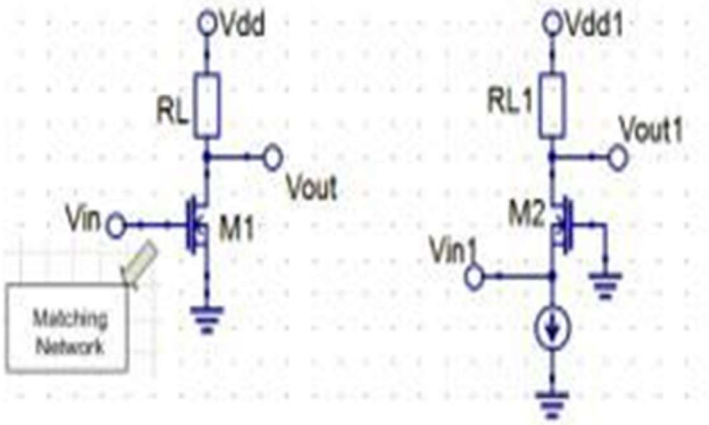

Fig: CMOS Low Noise Amplifier

The easiest way to tell if a FET is common source, common drain, or common gate is to examine where the signal enters and leaves. the configuration of cs amplifier is the input being a voltage between the gate and ground, and the output being a voltage between the drain and ground in electronics common-source amplifier is one of three basic single-stage field effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. The easiest way to tell if a FET is common source, Common drain or common gate is to examine where the signal enters and leaves. The remaining terminal is what is known as "common".

In this example, the signal enters the gate, and exits the drain. The only terminal remaining is the source. This is a common-source FET circuit. The analogous bipolar junction transistor circuit may be viewed as a transconductance amplifier or as a voltage amplifier. As a transconductance amplifier, the input voltage is seen as modulating the current going to the load. As a voltage amplifier, input voltage modulates the current flowing through the FET, changing the voltage across the output resistance according to Ohm's Law.

Catalyst Research Volume 23, Issue 2, September 2023 Pp. 1165-1171

Proposed Design:

CMOS has no static power when switching does not take place. But the semiconductor devices conduct or leak through the reverse biased channels and provide a path from VDD to ground and this constitutes static power consumption. There are various sources of leakage currents and we will be explaining the primary sources.

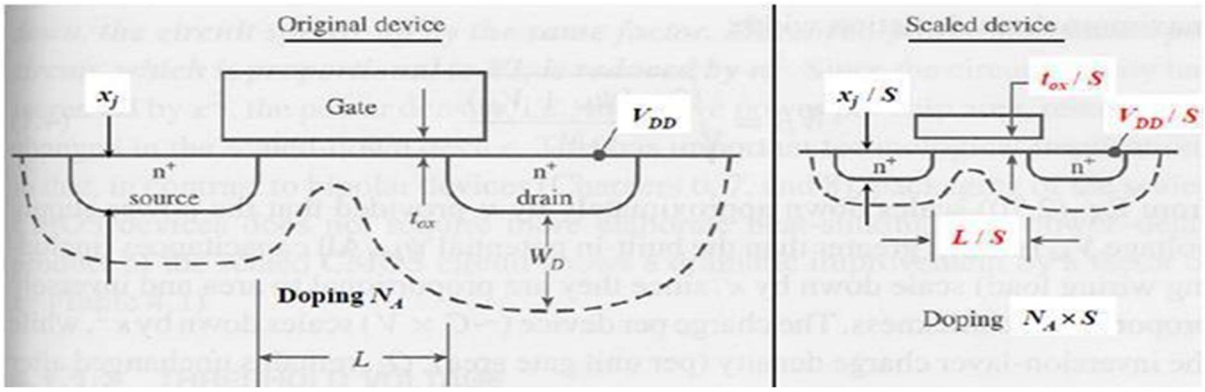

Fig: Scaling of Transistor Dimensions

The proposed wideband low noise amplifier consisting of two stages. In the first stage, a commongate topology is combined with the dual-resonance matching network technique, which results in wideband matching at the input stage. As it is known, the common-gate structure improves the input matching property of the LNA structure. In the proposed structure, on the one hand, the first frequency point has been generated by resonating between the inductor LS and Cgs1. On the other hand, the second frequency point has been generated by resonating between two pair frequency points, Lg2 and Cgs2 as a strong frequency point, and LD1 and the resulted capacitance of CD to CM4. The combination of these frequency points greatly improves the input matching at the whole of the frequency range. In addition, a resistor (Ro) is connected between the source and drain of M1 to be parallel to the channel length modulation resistance of M1, which is used to control the gain and input matching. The current-bleeding technique with diode-connected load is adopted to inject more current leading to increase voltage gain and decrease NF. In the output, the CS–CD currentreuse technique is applied.

A common source (CS) cascode LNA is the preferred choice among the different topologies, due to its good linearity, better input matching, along with high gain and low noise figure with the lowest power consumption. Figure 1 shows the basic circuit diagram of the common source cascode LNA. The degenerated inductor Ls in combination with the gate-to source capacitance (Cgs) of the driving transistor (M1) produces the real part of the input impedance, while the inductor Lg adds a degree of freedom to set the desired frequency of operation (0) .

Catalyst Research Volume 23, Issue 2, September 2023 Pp. 1165-1171

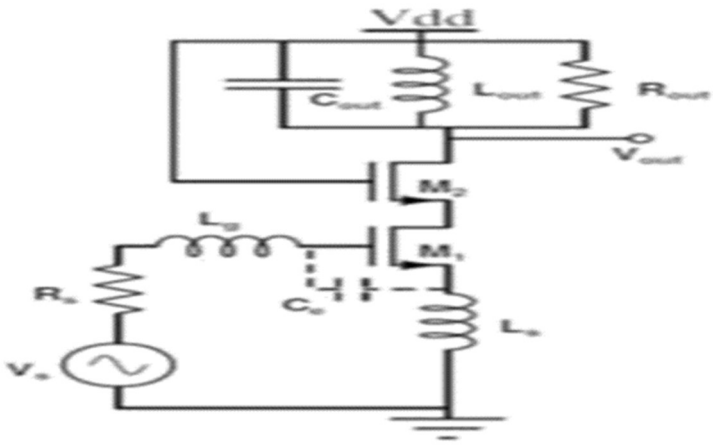

Fig: Proposed CMOS Cascode LNA

The drain current of a MOS device in the submicron region with short-channel effects such as velocity saturation, channel length modulation, etc., operating in different regions can be described. For the noise analysis, an equivalent small-signal circuit to Fig. 4.1 is shown in Fig. 4.2 Here, four noise current sources are considered: in, RS (the thermal noise current due to RS), in, Rout (the thermal noise current due to Rout).

Simulation Results:

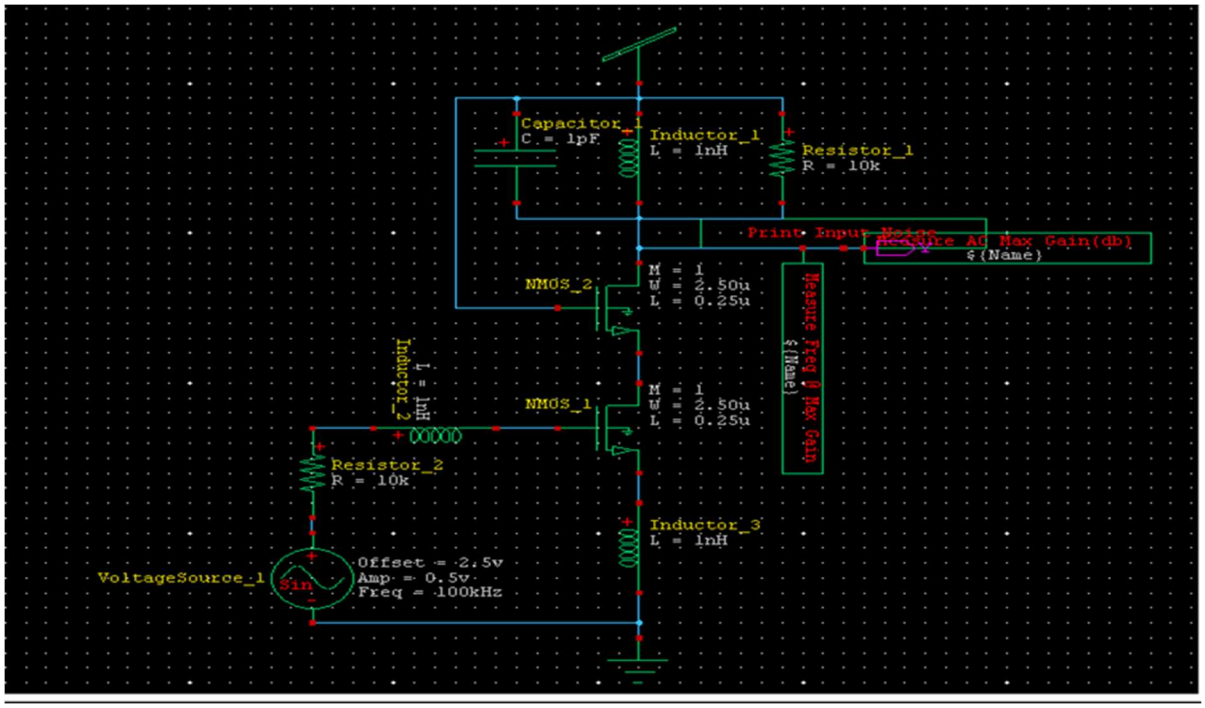

Fig: CS Cascode Low Noise Amplifier

Catalyst Research Volume 23, Issue 2, September 2023 Pp. 1165-1171

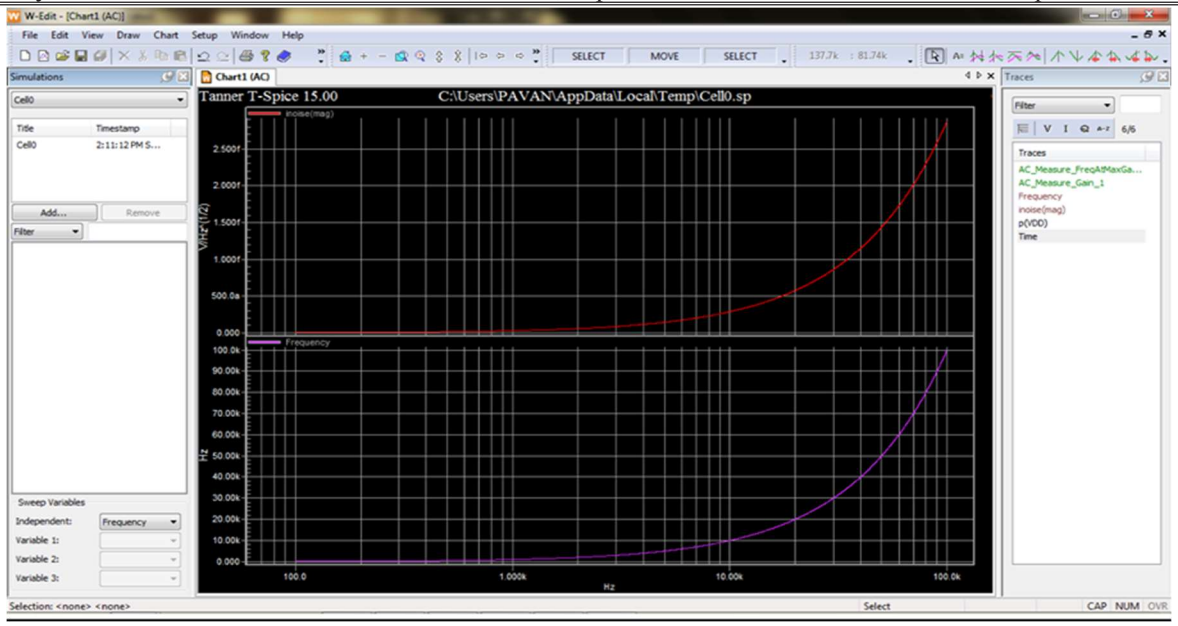

Fig: Simulation result for CS Cascode Low Noise Amplifier

Type Of LNA	Tech	Noise Figure (DB)	IIP3 (DBM)	Av (Db)	Power (po)	Supply (VDD)
Transconductance LNA	130nm Cmo s	2.7db@ 2MHZ	-4dBm	17dB	25mw	1.8V
Ultra Wideband LNA	180nm Cmos	3.35db@ 50MHZ	-3dBm	12.35dB	9.52mw	1V
Cascode With Inductor Based Cmos LNA	130nm Cmos	4.5db 50MHZ	-2dBm	25db	0.4mw	1V
Current Reuse Inductive degenerative cascode CMOS LNA	90nm Cmos	5db@ 2.4GHZ	-18dBm	14.5db	90µm	0.8V

Conclusion:

Previously we verified different types of Low power LNA's like Cascode inductive LNA, Ultra wide band LNA and Transconductance LNA but each has its own constraints like noise figure and gain. For that reason we proposed "current reuse inductively degenerated cascade CMOS LNA"

which have better gain of 14.3dB and a noise figure of 5dB with a very less power consumption about 90µ by applying "0.8v"supply. And also we verified that less channel length technology node independently depends on power consumption. So we designed this model as current reuse technique, which greatly reduces power consumption at 2.4GHZ LNA input in 90nm CMOS technology node.

References:

[1]. Dumesnil, E., Nabki, F., and Boukadoum, M. (2014). « RF-LNA circuit synthesis by genetic algorithm-specified artificial neural network. In 2014 21st IEEE international conference on electronics, circuits and systems (ICECS) (pp. 758–761).
[2]. Rahnama, M., Gilmalek, Y. M., and Kordalivand, A. M. (2010).Ultra wide-band LNA using RFCMOS technology and tunabilityband with neural network. In 2010 IEEE control and system graduate research colloquium (ICSGRC) (pp. 75–79).
[3]. Enz, C. C., &Vittoz, E. A. (2006). Charge-based MOS transistor modeling. Chichester: Wiley.
[4] .Tsividis, Y. (1999). Operation and modeling of the MOS transistor (2nd ed.). New York: Mc-Graw Hill.
[5]. Vittoz, E. A., &Fellrath, J. (1977). CMOS analog integrated circuits based on weak inversion operation. IEEE Journal of Solid-State Circuits, 12(3), 224–231.
[6]. Song, I., & Park, B.-G. (2008). A simple figure of merit of RF MOSFET for low-noise amplifier design. IEEE Electron Device Letters, 29(12), 1380–1382.
[7]. Shameli, A., Heydari, P. (2004). Ultra-low power RFIC design using moderately inverted MOSFETs: An analytical/experimental study, RFCI.
[8]. Mangla, A., Chalkiadaki, M.-A., Fadhuile, F., Taris, T., Deval, Y., &Enz, C. C. (2013). Design methodology for ultra low-power analog circuits using next generation BSIM6 MOSFET compact model. Microelectronics Journal, 44(7), 570–575.
[9]. Deen, M. J., Chen, C.-H., Asgaran, S., Rezvani, G., Tao, J., & Kiyota, Y. (2006). High frequency noise of modern MOSFETs Compact modeling and measurement issues. IEEE Transactions on Electron Devices, 53(9), 2062–2081.
[10]. Ng, T. C., Swe, T. N., Yeo, K.-S., Chew, K. W., Ma, J.-G., & Do, M. (2001). Small signal model and efficient parameter extraction technique for deep submicron MOSFETs for RF applications. IEEE Proceedings of Circuits Devices Systems, 148(1), 35–39.
[11]. Enz, C. C., & Cheng, Y. (2000). MOS transistor modeling for RF IC design. IEEE Journal of Solid-State Circuits, 35(2), 186–201.
[12] Y. S. Lin, C. Z. Chen, H. Y. Yang et al., "Analysis and design of a CMOS UWB LNA with dual-RLC-branch wideband input matching network," IEEE Transactions on Microwave Theory andTechniques,vol.58,no.2,pp.287–296,2010.
[13] A.I.A.Galal,R. K.Pokharel ,H.Kanay, andK. Yoshida," Ultrawideband low noise amplifier with shunt resistive feedback in 0.18 m CMOS process," in Proceedings of the 10th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF'10),pp.33–

Catalyst Research Volume 23, Issue 2, September 2023 Pp. 1165-1171

36,January2010.
[14] K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, and K. Yoshida, “A 2–16GHz CMOS current reuse cascaded ultrawidebandlownoiseamplifier,”inProceedingsoftheSaudiInternationalElectronics,CommunicationsandPhotonicsConference (SIECPC’11),April2011.
[15] K. Yousef, H. Jia, R. Pokharel, A. Allam, M. Ragab, and K. Yoshida, “Design of 3D Integrated Inductors for RFICs,” in Proceeding of 2012 Japan Egypt Conference on Electronics, Communications and Computers (JECECC’12),pp.22–25.
[16] X. N. Wang, X. L. Zhao, Y. Zhou, X. H. Dai, and B. C. Cai, “Fabrication and performance of novel RF spiral inductors on silicon,” Microelectronics Journal, vol. 36, no. 8, pp. 737–740, 2005.
[17] A. M. Niknejad and R. G. Meyer, “Analysis, design, and optimization of spiral inductors and transformers for Si RF IC’s,” IEEE Journal of Solid-State Circuits, vol. 33, no. 10, pp. 1470–1481,1998.
[18]T.H.Lee, The Design of CMOS Radio-Frequency Integrated Circuits,CambridgeUniversityPress,2ndedition,2004.
[19] S. S. Mohan, M. Del Mar Hershenson, S. P. Boyd, and T. H. Lee, “Bandwidth extension in CMOS with optimized on-chip inductors, ”IEEEJ ournalofSolid StateCircuits,vol.35,no.3,pp. 346–355,2000.
[20] H. T. Friis, “Noise figure of radio receivers, ”Proceedings of the IRE,vol.32,no.7,pp.419–422,1944.
[21] H.Y.TsuiandJ.Lau, “Experimental results and diearea efficient self-shieldedon chipvertical solenoid inductors formulti-GHz CMOS RFIC,” in Proceedings of the IEEE Radio Frequency Integrated Circuits(RFIC)Symposium,pp.243–246,June2003.